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Asynchronous FIFO DESIGN

(Clock Domain crossing)

Explained in detail.

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Design **Why a flip flop have
setup time and hold time?**

Explained!

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work. Bring observation,
manual, pen etc, with you.
Make sure that your hands
are clean and dry when you
use the computer.

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Integration, VLSI-SoC 2015, held in Daejeon, Korea, in October 2015. The 10 papers included in the book were carefully reviewed and selected from the 44 full papers presented at the conference. The papers cover

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a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about new challenges both at the

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physical and system-design levels, as well as in the test of these systems.

This book is structured as a step-by-step course of study along the lines of a VLSI integrated circuit design

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project. The entire Verilog language is presented, from the basics to everything necessary for synthesis of an entire 70,000 transistor, full-duplex serializer-deserializer, including synthesizable PLLs. The

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author includes everything
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downloadable files that accompany the book. For readers with access to appropriate electronic design tools, all solutions can be developed, simulated, and synthesized as described in the book. A partial list

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of design topics includes
design partitioning,
hierarchy decomposition,
safe coding styles, back
annotation, wrapper modules,
concurrency, race
conditions, assertion-based
verification, clock

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synchronization, and design for test. A concluding presentation of special topics includes System Verilog and Verilog-AMS.

This book provides step-by-step guidance on how to

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design VLSI systems using Verilog. It shows the way to design systems that are device, vendor and technology independent. Coverage presents new material and theory as well as synthesis of recent work

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with complete Project Designs using industry standard CAD tools and FPGA boards. The reader is taken step by step through different designs, from implementing a single digital gate to a massive

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design consuming well over 100,000 gates. All the design codes developed in this book are Register Transfer Level (RTL) compliant and can be readily used or amended to suit new projects.

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This book introduces readers to a variety of tools for analog layout design automation. After discussing the placement and routing problem in electronic design automation (EDA), the

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authors overview a variety of automatic layout generation tools, as well as the most recent advances in analog layout-aware circuit sizing. The discussion includes different methods for automatic placement (a

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template-based Placer and an optimization-based Placer), a fully-automatic Router and an empirical-based Parasitic Extractor. The concepts and algorithms of all the modules are thoroughly described, enabling readers

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to reproduce the methodologies, improve the quality of their designs, or use them as starting point for a new tool. All the methods described are applied to practical examples for a 130nm design

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process, as well as placement and routing benchmark sets.

This book, and the research it describes, resulted from a simple observation we made sometime in 1986. Put

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simply, we noticed that many VLSI design tools looked "alike". That is, at least at the overall software architecture level, the algorithms and data structures required to solve problem X looked much like

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those required to solve problem X'. Unfortunately, this resemblance is often of little help in actually writing the software for problem X' given the software for problem X. In the VLSI CAD world,

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technology changes rapidly enough that design software must continually strive to keep up. And of course, VLSI design software, and engineering design software in general, is often exquisitely sensitive to

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some aspects of the domain (technology) in which it operates. Modest changes in functionality have an unfortunate tendency to require substantial (and time-consuming) internal software modifications. Now,

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observing that large engineering software systems are technology dependent is not particularly clever. However, we believe that our approach to xiv Preface dealing with this problem took an interesting new

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direction. We chose to investigate the extent to which automatic programming ideas could be used to synthesize such software systems from high-level specifications. This book is one of the results of that

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effort.

This book is based on the 18 tutorials presented during the 26th workshop on Advances in Analog Circuit Design. Expert designers present readers with

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information about a variety of topics at the frontier of analog circuit design, with specific contributions focusing on hybrid ADCs, smart sensors for the IoT, sub-1V and advanced-node analog circuit design. This

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book serves as a valuable reference to the state-of-the-art, for anyone involved in analog circuit research and development.

In some places, the order of presentation has been

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changed to fine-tune the book's effectiveness as a senior and graduate-level teaching text. Fabrication principles covered include those for such circuits as CMOS, BIPOLAR, BICMOS, FET, and more.

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This book was motivated by the problems being faced with shrinking IC process feature sizes. It is well known that as process feature sizes shrink, a host of electrical problems such

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as cross-talk, electromigration, self-heat, etc. become important. Cross-talk is one of the major problems since it results in unpredictable design behavior. In particular, it can result in significant

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delay variation or signal integrity problems in a wire, depending on the state of its neighboring wire. Typical approaches to tackling the cross-talk problem attempt to fix the problem once it is created.

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This book introduces a framework for cross-talk-free IC design. The main foundation of the book is the use of a predetermined layout pattern on the IC, which we call a 'layout fabric'. The authors

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characterize this fabric and show how it yields cross-talk-immune designs. Two VLSI design flows are introduced which use the fabric concept. One flow is a minimally modified standard-cell based flow.

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The other flow uses a network of PLAs to implement the circuit. The authors also introduce 'wire removal' techniques which improve circuit wire ability and thereby reduce circuit area. The new concepts

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presented here will be of interest to IC designers and researchers.

The purpose of this introductory book is to couple the teaching of chaotic circuit and systems

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theory with the use of field programmable gate arrays (FPGAs). As such, it differs from other texts on chaos: first, it puts emphasis on combining theoretical methods, simulation tools and physical realization to

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help the reader gain an intuitive understanding of the properties of chaotic systems. Second, the "medium" used for physical realization is the FPGA. These devices are massively parallel architectures that

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can be configured to realize a variety of logic functions. Hence, FPGAs can be configured to emulate systems of differential equations. Nevertheless maximizing the capabilities of an FPGA requires the user

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to understand the underlying hardware and also FPGA design software. This is achieved by the third distinctive feature of this book: a lab component in each chapter. Here, readers are asked to experiment with

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computer simulations and FPGA designs, to further their understanding of concepts covered in the book. This text is intended for graduate students in science and engineering interested in exploring

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implementation of nonlinear dynamical (chaotic) systems on FPGAs.

The field of CMOS integrated circuits has reached a level of maturity where it is now a mainstream technology for

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high-density digital system designs. This volume deals with circuit design in an integrated CMOS environment. Emphasis is placed on understanding the operation, performance, and design o

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